MICRO NETWORKS

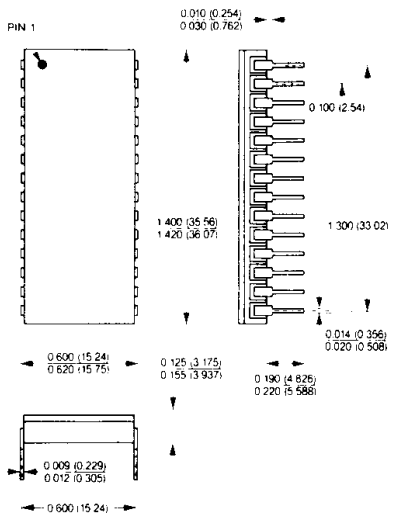
MN6227
MN6228

WIDEBAND, SAMPLING
12-Bit A/D
CONVERTERS

FEATURES

- **33kHz Sampling Rate With Internal T/H Amplifier**
- **16.5kHz Full-Power Input Bandwidth**
- **70dB Signal-to-Noise Ratio Over Full Bandwidth**
- **−80dB Harmonics Over Full Bandwidth**
- **Full 8 or 16-Bit μP Interface: CS, CE, R/C, A_0, 12/8 150nsec Bus Access Time**
- **Industry-Standard MN574A Package and Pinout**
- **1100mW Max Power**
- **Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)**

28 PIN DIP



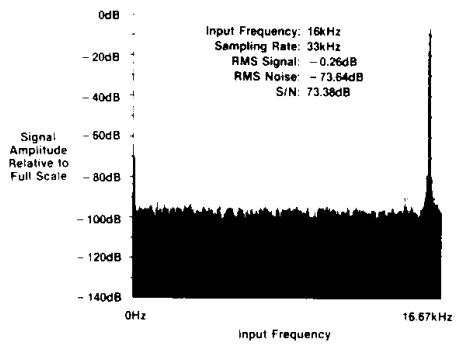
Dimensions in Inches
(millimeters)

DESCRIPTION

MN6227 and MN6228 are the first, general-purpose, high-speed, 12-bit, sampling A/D converters designed and specified for contemporary DSP applications in the fields of spectrum analysis, voice recognition, vibration analysis, signature recognition, and others. These devices consist of high-speed (25μsec), μP interfaced (CS, CE, read/convert, 3-state buffer, etc.), successive-approximation type, 12-bit A/D converters with internal, high-speed, track-hold (T/H) amplifiers. They have the ability to accurately sample and digitize transient or periodic input signals with slew-rate and frequency content orders of magnitude higher than can be converted by an A/D without a companion T/H.

MN6227 (10V input span) and MN6228 (20V input span) are configured in a manner that makes the T/H transparent to the user. There are no confusing acquisition time, aperture delay, or aperture jitter specifications. These are true sampling, broadband A/D converters that are specified accordingly. Sampling rate, analog-input full-power bandwidth, harmonic distortion, and signal-to-noise ratio (SNR, rms-to-rms) are all fully specified. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's (see sample spectrum below).

These devices are packaged in small, low-profile, 28-pin, side-brazed, ceramic DIP's and have the industry-standard MN574A pinout. Devices are fully specified for 0°C to +70°C (J and K models) or −55°C to +125°C (S and T models) operation.



May 1988

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN6227 MN6228 WIDEBAND SAMPLING 12-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6227J, K; MN6228J, K	0°C to +70°C
MN6227S, S/B, T, T/B	−55°C to +125°C
MN6228S, S/B, T, T/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 7)	0 to +16.5 Volts
Negative Supply (−Vcc, Pin 11)	0 to −16.5 Volts
Logic Supply (+Vdd, Pin 1)	0 to +7 Volts
Digital Inputs (Pins 2-6)	−0.5 to (+V_{dd} +0.5) Volts
Analog Inputs: Pins 10 and 12	±15 Volts
Pin 13 (MN6227)	±15 Volts
Pin 14 (MN6228)	±15 Volts
Analog Ground (Pin 9) to Digital Ground (Pin 15)	±1 Volt
Ref Out (Pin 8) Short Circuit Duration	Continuous to Ground

ORDERING INFORMATION

PART NUMBER — MN6227T/B

Select MN6227 or MN6228

Select suffix J, K, S, or T for desired performance and specified temperature range.

Add "/B" to "S" or "T" models for Environmental Stress Screening.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±V_{CC} = ±15V, +V_{dd} = +5V unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: MN6227		0 to +10, ±5		Volts
MN6228		±10		Volts
Input Impedance (Note 16): Resistance	1	5		Mohm
Capacitance		50		pF
Input Bias Current Over Full Temperature Range (Note 16):		±100	±600	nA
DIGITAL INPUTS CE, CS, R/C, A_0, 12/8				
Logic Levels: Logic "1"	+2.4			Volts
Logic "0"			+0.8	Volts
Loading: Logic Currents		±1	±10	μA
Input Capacitance (Note 16)		5		pF
DIGITAL OUTPUTS DBO — DB11, STS				
Output Coding (Note 2): Unipolar Ranges		Straight Binary		
Bipolar Ranges		Offset Binary		
Logic Levels: Logic "1" (I_{source} ≤ 320μA)	+2.4			Volts
Logic "0" (I_{sink} ≤ 1.6mA)			+0.4	Volts
Leakage (DBO—DB11) in High-Z State		±1	±10	μA
Output Capacitance (Note 16)		5		pF
INTERNAL REFERENCE				
Reference Output (Pin 8): Voltage	+9.9	+10	+10.1	Volts
Drift (Note 16)		±15		ppm/°C
Output Current (Notes 3, 16)			1	mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±V_{CC} Supplies	±14.5	±15	±15.5	Volts
+V_{dd} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection (Note 14): +V_{CC} Supply	−50			dB
−V_{CC} Supply	−50			dB
+V_{dd} Supply	−50			dB
Current Drains: +V_{CC} Supply		+22	+28	mA
−V_{CC} Supply		−34	−40	mA
+V_{dd} Supply		+9	+15	mA
Power Consumption		885	1095	mW

PERFORMANCE SPECIFICATIONS (Typical at T_A = +25°C, $\pm V_{CC}$ = ±15V, $+V_{dd}$ = +5V unless otherwise indicated)

DYNAMIC CHARACTERISTICS	MN6227J MN6228J	MN6227K MN6228K	MN6227S MN6228S	MN6227T MN6228T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	33	33	33	33	kHz
Maximum A/D Conversion Time (Note 5)	25	25	25	25	μsec
Signal-to-Noise Ratio (SNR, Note 6):					
Initial (+25°C) (Minimum)	68	70	68	70	dB
T_{min} to T_{max} (Minimum, Note 7)	66	68	66	68	dB
Harmonics and Spurious Noise (Note 8):					
Initial (+25°C) (Minimum)	−77	−80	−77	−80	dB
T_{min} to T_{max} (Minimum, Note 7)	−74	−77	−74	−77	dB
Input Signal Full-Scale Bandwidth (Minimum, Note 9)	16.5	16.5	16.5	16.5	kHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C) (Maximum)	±1	±½	±1	±½	LSB
T_{min} to T_{max} (Maximum, Note 7)	±1	±½	±1	±1	LSB
Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C)	11	12	11	12	Bits
T_{min} to T_{max} (Note 7)	11	12	11	12	Bits
Unipolar Offset Error (Notes 10, 11):					
Initial (+25°C) (Maximum)	±2	±2	±2	±2	LSB
Drift (Maximum)	±10	±5	±10	±5	ppm of FSR/°C
Maximum Change to T_{min} or T_{max} (Notes 7, 15)	±2	±1	±4	±2	LSB
Bipolar Zero Error (Notes 10, 12):					
Initial (+25°C) (Maximum)	±4	±4	±4	±4	LSB
Drift (Maximum)	±15	±10	±15	±10	ppm of FSR/°C
Maximum Change to T_{min} or T_{max} (Notes 7, 15)	±3	±2	±6	±4	LSB
Full Scale Accuracy Error (Notes 10, 13):					
Initial (+25°C) (Maximum)	±0.2	±0.1	±0.2	±0.1	%FSR
T_{min} to T_{max} Without Initial Adjustment	±0.4	±0.2	±0.7	±0.4	%FSR
T_{min} to T_{max} With Initial Adjustment	±0.2	±0.1	±0.5	±0.3	%FSR
Drift (Maximum)	±50	±25	±50	±25	ppm of FSR/°C
Maximum Change to T_{min} or T_{max} (Notes 7, 15)	±10	±5	±20	±10	LSB

SPECIFICATION NOTES:

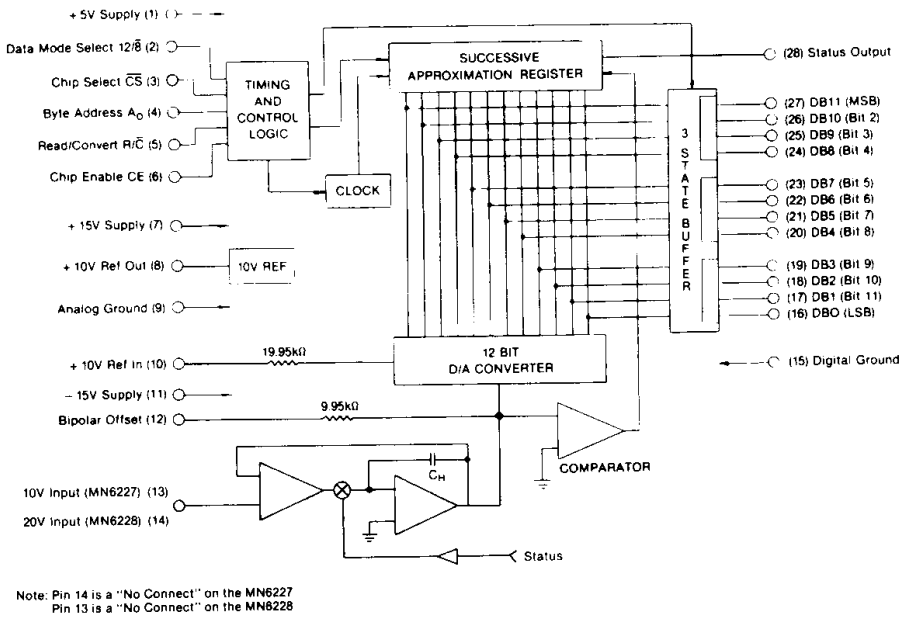
1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. See table of transition voltages in section labeled Digital Output Coding.
3. If the internal reference is used to drive an external load, the load should not change during a conversion.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 33kHz rate. Obviously, devices may be operated at lower sampling frequencies if desired and typically will meet all performance specs while sampling at rates of 40kHz or higher.
5. Whenever the Status Output (pin 28) is low (logic "0"), the internal T/H is in the track mode and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input sine wave (0db) at any frequency up to 16.5kHz.
7. MN6227J, K and MN6228J, K are fully specified for 0°C to +70°C operation. MN6227S, S/B, T, T/B and MN6228S, S/B, T, T/B are fully specified for −55°C to +125°C operation.
8. This parameter represents the peak signal to peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
9. This is the highest-frequency, full-scale, input signal for which the SNR and harmonic figures are guaranteed when sampling at a 33kHz rate.
10. Adjustable to zero with external potentiometer.
11. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 to 0000 0000 0001 when operating the MN6227 on its unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
12. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000 when operating the MN6227/6228 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding. Listed specs assume fixed 50Ω resistors between Ref Out (pin 8) and Ref In (pin 10) and between Ref Out (pin 8) and Bipolar Offset (pin 12).
13. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1110 to 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 to 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding. Listed specs assume fixed 50Ω resistors between Ref Out (pin 8) and Ref In (pin 10) and between Ref Out (pin 8) and Bipolar Offset (pin 12).
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or 0000 0000 0000 to 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
15. Listed maximum change specifications for unipolar offset, bipolar zero and full-scale accuracy correspond to the maximum change from the initial value (+25°C) to the value at T_{min} or T_{max}.
16. These parameters are listed for reference only and are not tested.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

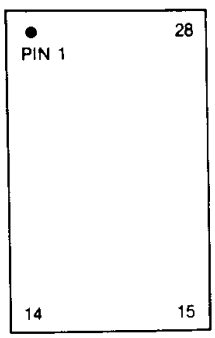
Part Number	Input Voltage Range		Specified Temperature Range	No Missing Codes	Integral Linearity	Minimum Sampling Rate	Minimum Input Bandwidth	SNR	Harmonics
	Unipolar	Bipolar							
MN6227J	0 to +10V	±5V	0°C to +70°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6227K	0 to +10V	±5V	0°C to +70°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6227S	0 to +10V	±5V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6227S/B	0 to +10V	±5V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6227T	0 to +10V	±5V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6227T/B	0 to +10V	±5V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6228J	N.A.	±10V	0°C to +70°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6228K	N.A.	±10V	0°C to +70°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6228S	N.A.	±10V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6228S/B	N.A.	±10V	−55°C to +125°C	11 Bits	±1 LSB	33kHz	16.5kHz	68dB	−77dB
MN6228T	N.A.	±10V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB
MN6228T/B	N.A.	±10V	−55°C to +125°C	12 Bits	±½ LSB	33kHz	16.5kHz	70dB	−80dB

BLOCK DIAGRAM



Note: Pin 14 is a "No Connect" on the MN6227
Pin 13 is a "No Connect" on the MN6228

PIN DESIGNATIONS



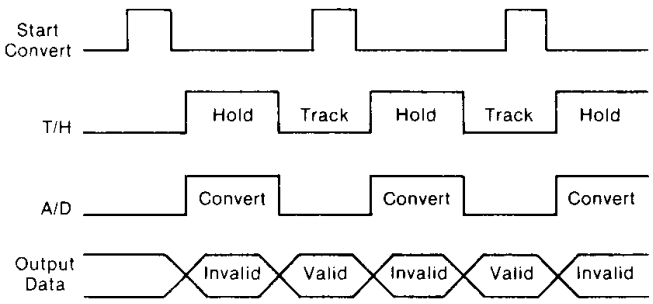
(1)	+5V Supply (+V_{dd})	(28)	Status Output
(2)	Data Mode Select 12/8̄	(27)	DB11 (MSB)
(3)	Chip Select CS̄	(26)	DB10 (Bit 2)
(4)	Byte Address A_0	(25)	DB9 (Bit 3)
(5)	Read/Convert R/C̄	(24)	DB8 (Bit 4)
(6)	Chip Enable CE	(23)	DB7 (Bit 5)
(7)	+15V Supply (+V_{cc})	(22)	DB6 (Bit 6)
(8)	+10V Ref Out	(21)	DB5 (Bit 7)
(9)	Analog Ground	(20)	DB4 (Bit 8)
(10)	+10V Ref In	(19)	DB3 (Bit 9)
(11)	−15V Supply (−V_{cc})	(18)	DB2 (Bit 10)
(12)	Bipolar Offset	(17)	DB1 (Bit 11)
(13)	Analog Input MN6227 (N.C. MN6228)	(16)	DB0 (LSB)
(14)	Analog Input MN6228 (N.C. MN6227)	(15)	Digital Ground

DESCRIPTION OF OPERATION

MN6227 and MN6228 are complete, 12-bit A/D converters with internal microprocessor-interface logic and internal track-hold (T/H) amplifiers. They have been designed to repetitively sample and digitize dynamically changing input signals in DSP-type applications. The A/D-converter sections of these devices employ the successive-approximation (SA) conversion technique, and A/D's of this type, while offering excellent tradeoffs in terms of speed, resolution, and power consumption, are nortoriously poor in their ability to accurately convert dynamically changing (slewing) analog-input signals. In fact, the A/D converter section of the MN6227/6228 has a 25μsec conversion time, and if it did not have a T/H, it would be effectively incapable of accurately digitizing a signal slewing more than ± ½ LSB during that period. This corresponds to an input slew-rate limit of ± 0.098mV/μsec (for a device with a ± 10V input range) or a full-scale, sinusoidal, input bandwidth of 1.56Hz. The input bandwidth of MN6227/6228 is increased more than 4 orders of magnitude by its internal T/H amp. When these converters are commanded to perform a conversion, the T/H instantaneously "freezes" the input signal and holds it constant while the A/D converter performs a conversion.

The T/H is configured in such a manner as to be transparent to the user. A high-impedance input buffer isolates it from the external signal source, and its output is internally connected directly to the A/D. Its operational state is controlled by the A/D in the sense that whenever the A/D is performing a conversion (Status Line = "1"), the T/H is driven into its hold mode, and when the A/D is between conversions (Status Line = "0"), the T/H is in its track (signal acquistion) mode.

MN6227/6228 TIMING



When the A/D is not converting and the T/H is acquiring a new signal, digital output data from the previous conversion is valid and ready to be read.

MN6227/6228 are designed such that when conversions are initiated at any rate up to 33kHz, enough time remains between the falling edge of Status and the next Start Convert command for the T/H to fully acquire its next sample. When the device is clocked at a 33kHz sampling rate, the T/H has the ability to accurately acquire, track, and hold full-scale input signals with frequency components up to 16.5kHz. In most DSP-type applications, MN6227/6228 will be required to repetitively sample and digitize input signals with frequencies below 16.5kHz. This will ensure that the Nyquist criterion of sampling 2 times per period is achieved. Similarly, it ensures that the sampling (and digitizing) frequency (33kHz) is at least 2 times the signal frequency.

In most applications, MN6227/6228 will require only power supplies, bypass capacitors, and two fixed resistors to provide the complete sampling/conversion function. The completeness of the device makes it most convenient to think of MN6227/6228 as a function block with specific input/output and transfer characteristics, and it is quite unnecessary to concern oneself with its inner workings.

Operating MN6227/6228 under microprocessor control (it also functions as a stand-alone A/D) will consist, in most applications, of a series of read and write operations. Initiating a conversion involves sending a command from the processor to the A/D and is essentially a write operation. Retrieving digital output data is accomplished with read operations. Once the proper signals have been received and a conversion has begun, it cannot be stopped or restarted, and digital output data is not available until the conversion has been completed. Immediately following the initiation of a conversion cycle, the MN6227/6228's Status Line (also called Busy Line or End of Conversion (E.O.C.)) will rise to a logic "1" indicating that a conversion is in progress. At the end of a conversion, the internal control logic will drop the Status Line to a "0" and enable internal circuitry to permit output data to be read by external command. By sensing the state of the Status Line or by waiting an appropriate amount of time, the microprocessor will know when the conversion is complete and that output data is valid and can be read.

If MN6227/6228 is to be operated with 12-bit or greater microprocessors, all 12 output bits can be 3-state enabled simultaneously permitting data collection with a single read operation. If MN6227/6228 is operated with an 8-bit μP, output data can be formatted to be read in two 8-bit bytes. The first will contain the 8 most significant bits (MSB's). The second will contain the remaining 4 least significant bits (LSB's) in a left justified format with 4 trailing "0's".

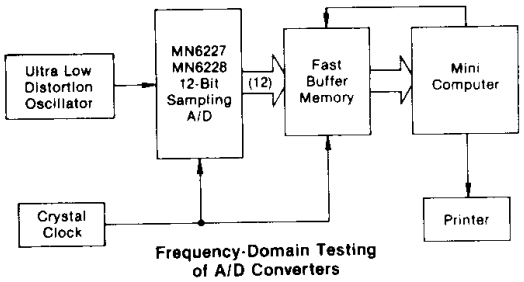
THE INTERNAL T/H AMPLIFIER

As stated earlier, MN6227/6228's internal T/H amplifier is configured in such a way as to be transparent to the user. The T/H's output is connected directly to the input of the A/D converter, and its operational mode is controlled directly by the Status output of the A/D converter. Consequently, users of MN6227/6228 need not burden themselves with oftentimes confusing T/H specifications like acquisition time, aperture-delay time, aperture jitter, droop rate, etc.. These parameters are not specified for MN6227/6228 and are, in fact, impossible to directly test considering that the T/H output and control lines are not accessible at the device pins. The manner in which MN6227/6228 is specified (input bandwidth, sampling rate, signal-to-noise ratio, harmonic distortion, etc.) obviates the need for knowing the specific T/H time-domain performance specifications, however, we do supply typical values for critical T/H parameters on the following page.

Note that the static errors (gain error, track-mode offset error, and pedestal) of the T/H function add directly to the corresponding errors of the A/D converter but that both are effectively nulled with the functional laser trimming of the A/D. T/H offset error and pedestal, for example, add directly to A/D-converter offset error. However, when the A/D offset is functionally laser trimmed, it is done with the whole device sampling at a 33kHz rate and the T/H is in the hold mode whenever trimming is actually performed. Consequently, all error sources are compensated for. All static errors on MN6227/6228 (accuracy error, unipolar offset error, bipolar zero error, etc.) are tested and specified as full input-output transfer specifications and include both the T/H and A/D.

Typical T/H Performance Specifications	
Gain Error Gain Linearity Error	± 0.01% ± 0.005% FSR
Track-Mode Output Offset Error Pedestal	± 0.5mV ± 1mV
Acquisition Time: 10V step to ± 0.01% 20V step to ± 0.01% Track-Hold Transient Settling (to ± 1mV)	1μsec 2μsec 250nsec
Slew Rate Full Power Bandwidth	± 40V/μsec 500kHz
Effective Aperture Delay Time Aperture Jitter	– 25nsec 0.5nsec
Droop Rate Hold-Mode Feedthrough Attenuation	± 0.1μV/μsec – 80 dB

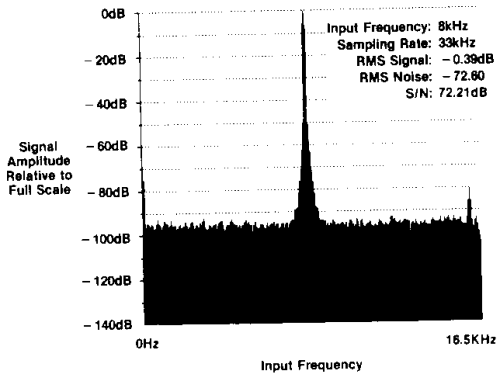
FREQUENCY-DOMAIN TESTING — MN6227/6228 is specified and tested statically in the traditional manner (linearity, accuracy, offset error, current drains, etc.) and dynamically in the frequency-domain. In the dynamic tests, MN6227/6228 is operated in a manner that resembles an application as a digital spectrum analyzer. A very low distortion signal generator (harmonics – 90dB) is used to generate a pure, full-scale, 16kHz sine wave that MN6227/6228 samples and digitizes at a 33kHz rate. These conditions (signal period = 62.5μsec, sampling interval = 30μsec) approach the Nyquist sampling limit (at least 2 samples per signal cycle; sampling frequency greater than 2 times signal frequency). A total of 512 sample-and-convert operations are performed, and the digital-output data is stored in a high-speed, FIFO, buffer-memory box. The 512 data points are then accessed by a microcomputer which executes a 512-point Fast Fourier Transform (FFT) after applying a Hanning (raised cosine) window function to the data. The resulting spectrum shows the amplitude and frequency content of the converted signal along with any errors (noise, harmonic distortion, spurious signals, etc.) introduced by the A/D converter. Subsequently, signal-to-noise ratio (SNR) and harmonic distortion measurements are read from the spectrum. A functional block diagram of the test setup appears below, and a sample spectrum appears above.



Frequency-Domain Testing of A/D Converters

The spectrum above is the real portion (imaginary portions of spectrums are discarded) of a 512-point FFT. The horizontal axis is the frequency axis, and its rightmost end is equal to ½ the sampling rate (16.5kHz in this case). The horizontal axis is divided into 256 frequency bins, each with a width of 64.45Hz. Recall that the highest frequency on the frequency axis of the spectrum of a sampled signal is equal to one-half the sampling rate and that input signals with frequencies higher than ½ the sampling rate are effectively "undersampled" and aliased back into the spectrum.

The vertical axis of the spectrum corresponds to signal amplitude in rms volts relative to a full-scale sinusoidal input signal (0dB). The sample spectrum above is the result of averaging 10 512-point FTT's run on data taken from an MN6227 operating on its bipolar input range (± 5V) with a full-scale input sine wave ($v(t) = 5\sin\omega t$) at a frequency of 8kHz. In the spectrum, the full-scale input signal appears at 8kHz at a



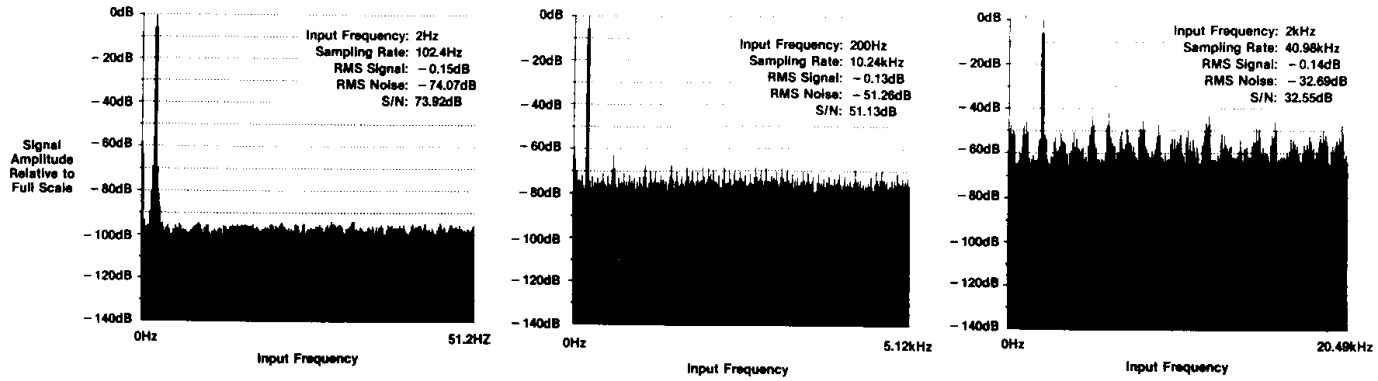
level of – 0.39dB. Full-scale rms signals do not appear at – 3dB levels because the FFT program has been normalized to bring them to zero. The d.c. component in the spectrum is effectively the offset error of the MN6227 combined with that of the signal generator and test fixture. A second harmonic, if it were either present in the input signal or created by the MN6227, would appear at 16kHz. If a third harmonic were present, it would be aliased back into the spectrum and appear at 9kHz. Harmonic distortion and spurious noise levels are calculated as the ratio (in dB) of the signal level to the strongest harmonic or spurious (nonharmonic) signal in the spectrum. In the sample spectrum above, the strongest harmonic is the second. It appears at a level of – 80.29dB, and the signal to harmonics ratio is equal to 79.9dB. Rms noise is calculated as the rms summation of all nonfundamental and nonharmonic components in the output spectrum, and SNR is calculated as the ratio of the rms signal to the rms noise. For the above spectrum, the normalized rms signal level is – 0.39dB; the rms noise level is – 72.60dB and the SNR is 72.21dB.

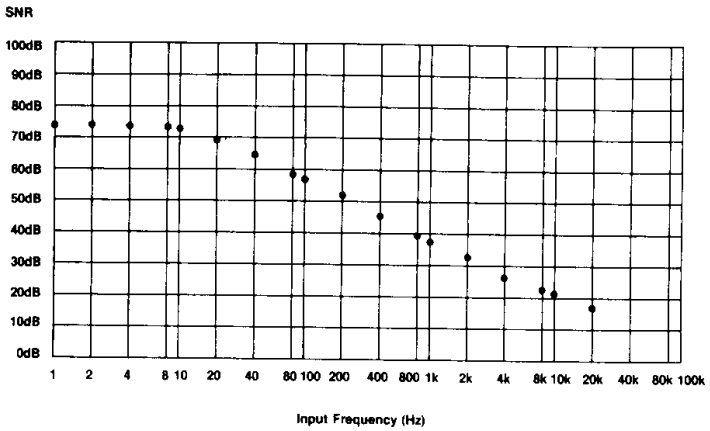
The term "noise" is generally used to describe what remains in the output spectrum after all fundamental, harmonic, d.c., and outstanding spurious components have been removed. It generally appears across all frequency bins at some relatively flat level sometimes referred to as the "noise floor". The rms noise, as described above, represents the broadband noise that would appear superimposed on the sinusoidal input signal if that signal were perfectly recreated from the stored digital-output data. Virtually all the noise in the output spectrum is created either by the act of digitizing or by the A/D converter itself.

In a simple, first-order analysis, the noise in the output spectrum of an A/D converter can be traced to three sources. All three of these noise sources have the potential to manifest themselves as quasi-random relative-accuracy errors in any single A/D conversion of a static signal and subsequently, the potential to manifest themselves as broadband noise in a series of conversions of a dynamically changing signal. Two of these noise sources (quantization noise and converter noise) are effectively constant and do not change with input-signal frequency. The third (aperture noise) usually varies linearly as a function of input-signal frequency, basically doubling whenever input frequency doubles.

Digitizing an analog signal quantizes it or "rounds it off". Digitizing or quantizing an analog signal with a 12-bit A/D effectively "rounds off" the signal to one of 4096 possible discrete levels. This rounding off produces an inherent accuracy error in that the digital output may no longer **exactly** represent the analog input. If one has an ideal A/D converter with all other accuracy-error sources driven to zero, the actual value of rounding-off error or quantization error can be as small as zero or as large as ± ½ LSB from conversion to conversion. In a single conversion of a static input signal,

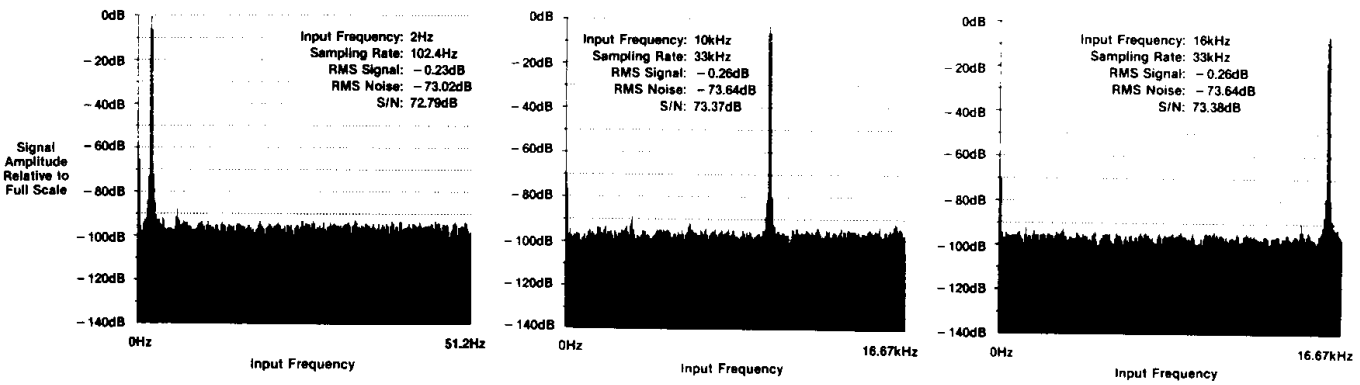
Effective Resolution vs. Input Frequency
MN574A, 25μsec, 12-Bit A/D

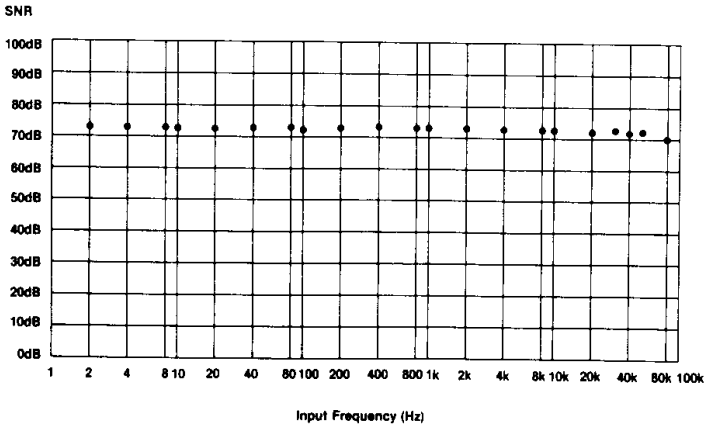




The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN574A type 12-bit A/D converter without a companion T/H amplifier. The input signal frequencies are respectively 2Hz, 200Hz, and 2kHz. The A/D's conversion time is approximately 25μsec; the sampling rates are respectively 102.4Hz, 10.24kHz, and 40.98kHz. The accompanying plot shows the rapid (6dB/octave) degradation of SNR (effective resolution) with increasing input frequency when SA type A/D converters are used to digitize dynamically changing input signals without the aid of a T/H amplifier.

Effective Resolution vs. Input Frequency
MN6227, 33kHz, 12-Bit, Sampling A/D





The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN6227 12-bit sampling A/D. The input signal frequencies are respectively 2Hz, 10kHz, and 16kHz, and the sample/convert rates are respectively 102.4Hz, 33.33kHz, and 33.33kHz. The accompanying plot shows that MN6227's internal T/H amplifier enables the device to maintain near ideal SNR independent of increasing input frequencies. The aperture jitter of the T/H is small enough to maintain SNR for undersampled input frequencies, i.e., for frequencies greater than 16.5kHz.

quantization error is simply an accuracy error. It is impossible for a given conversion of an unknown signal to be more accurate than ± ½LSB. In a series of conversions of a dynamically changing signal, actual instantaneous quantization error varies from sample to sample and manifests itself as broadband noise. In the output spectrum, this noise limits the theoretically achievable signal-to-noise ratio to the following:

$$\text{Ideal SNR} = (6.02n + 1.76)\text{dB}$$

$$n = \text{number of bits}$$

For an ideal 12-bit A/D, the theoretical noise floor in a 512-point FFT occurs around −98dB, and the theoretical SNR is 74dB. For an ideal 11-bit A/D and a 512-point FFT, the numbers are −92dB and 68dB respectively.

The second type of single-conversion accuracy error that manifests itself as broadband noise in the output spectrum results from the actual noise of the A/D converter. This "converter noise" is frequently referred to as "transition noise" and manifests itself, among other ways, by allowing certain fixed, static, input signals to produce either of two adjacent output codes from one conversion to the next. In most A/D converters, the transition from one given digital output code to the next (or vice versa) does not always occur at exactly the same analog input voltage. The "transition voltage" varies from conversion to conversion, and this "transition noise" (the band of adjacent-code uncertainty) is normally on the order of ± 1/10 to ± 1/3 LSB. It is caused by broadband noise and timing jitter in the A/D's constituent components (especially its comparator and reference circuit). In a single given A/D conversion, transition noise adds (or subtracts) to the device's static differential linearity error. Again, this phenomenon will manifest itself as an accuracy error in any single conversion and as noise in any series of conversions of a changing input signal.

This second noise component should be thought of simply as the "converter noise". Recall that quantization noise is a result of the digitizing process, and it limits SNR to some theoretical value. Its effect is independent of the type or kind of A/D converter used. Converter noise is a function of how "noisy" a selected A/D converter may be, and it reduces actual measured SNR's to a level something below ideal. Hence MN6227/6228 guarantees 70dB and not 74dB initial room-temperature SNR.

The third component of A/D converter noise derives from the fact that SA type A/D converters (without companion T/H amplifiers) cannot accurately convert dynamically changing input signals. Because of the nature of the technique of successive approximations, it is imperative that A/D's using this technique maintain a stable input signal during their conversion (aperture) time. Slew rates in excess of (± ½LSB) / (conversion time) can cause accuracy errors in any individual conversion. In a series of conversions of a sinusoidal signal, the slew rate varies from sample to sample, and the consequent aperture (slew-rate) errors manifest themselves as broadband noise.

This third component of A/D noise is effectively eliminated by MN6227/6228's internal T/H. The T/H's ability to instantaneously freeze the slewing input signal (limited only by the T/H's aperture jitter) and hold it constant results in the A/D seeing a series of d.c. signals and not the sinusoid itself. MN6227/6228's ability to maintain SNR over its full input bandwidth (up to the "Nyquist frequency" or ½ the sampling rate) is the result of the T/H's ability to limit the overall noise to the quantization noise plus the noise inherent in the A/D.

The plots on the previous page demonstrate that an A/D without a companion T/H is effectively incapable of accurately converting analog input signals above some critical frequency (slew rate) and that the A/D's SNR or "effective resolution" deteriorates at approximately 6dB/octave above that frequency. Basically, the A/D's quantization and converter noise remain constant while its aperture noise doubles each time the input frequency doubles.

MN6227/6228's internal T/H effectively eliminates aperture noise allowing the A/D to maintain "low-frequency SNR" as the actual input frequency increases.

APPLICATIONS INFORMATION

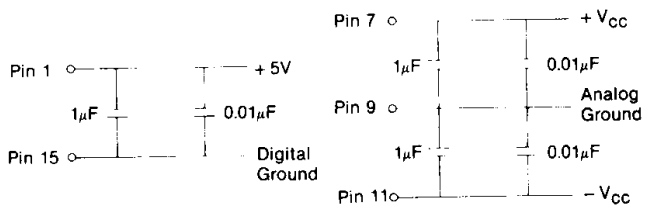
LAYOUT CONSIDERATIONS AND GROUNDING—Proper attention to layout and decoupling is necessary to obtain specified accuracy from the MN6227/6228. It is critically important that the device's power supplies be filtered, well-regulated, and free from high-frequency noise. Use of noisy supplies may cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output.

Decoupling capacitors should be used on all power-supply pins; the +5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (Digital Ground) and the $+V_{CC}$ and $-V_{CC}$ pins should be decoupled directly to pin 9 (Analog Ground). Suitable decoupling capacitors are 1μF tantalum type in parallel with a 0.1μF ceramic discs.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Pins 10 (Reference In), 12 (Bipolar Offset), and 13 and 14 (Analog Inputs) are particularly noise susceptible. Circuit layout should attempt to locate the MN6227/6228 and associated analog-input circuitry as far as possible from logic circuitry. The use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred. If external offset and gain adjust potentiometers are used, the pots and associated series resistors should be located as close to MN6227/6228 as possible. If no trim adjusting is required and fixed resistors are used, they likewise should be as close as possible.

Analog (pin 9) and Digital (pin 15) Ground pins are not connected to each other internal to MN6227/6228. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a nonpolarized 0.01μF ceramic bypass capacitor should be connected between pins 9 and 15 as close to the unit as possible and wide conductor runs employed. Pin 9 (Analog Ground) is the ground reference point for MN6227/6228's internal reference. It should be connected as close as possible to the analog input signal reference point.

POWER SUPPLY DECOUPLING



CONTROL FUNCTIONS—Operating MN6227/6228 under microprocessor control is most easily understood by examining the assorted control-line functions in a truth table. Table 1 below is a summary of MN6227/6228 control-line functions. Table 2 is the control-line Truth Table.

Table 1: MN6227/6228 Control Line Functions

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0→1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1→0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1→0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0→1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in 2 8-bit bytes, A_0 = "0" accesses 8 MSB's (high byte) and A_0 = "1" accesses 4 LSB's and trailing "0's" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line.

Unless Chip Enable (CE, Pin 6, logic "1" = active) and Chip Select ($\overline{CS}$, Pin 3, logic "0" = active) are both asserted, various combinations of logic signals applied to other control lines (R/$\overline{C}$, 12/$\overline{8}$, and A_0) will have no effect on MN6227/6228 operation. When CE and $\overline{CS}$ are both asserted; the signal applied to R/$\overline{C}$ (Read/Convert, Pin 5) determines whether a data read (R/$\overline{C}$ = "1") or a convert operation (R/$\overline{C}$ = "0") is initiated.

Table 2: MN6227/6228 Truth Table

CONTROL INPUTS					MN6227/6228 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	1→0	X	0	Initiates 12-Bit Conversion
1	0	1→0	X	1	Initiates 8-Bit Conversion
0→1	0	0	X	0	Initiates 12-Bit Conversion
0→1	0	0	X	1	Initiates 8-Bit Conversion
1	1→0	0	X	0	Initiates 12-Bit Conversion
1	1→0	0	X	1	Initiates 8-Bit Conversion
1	0	1	1	X	Enables 12-Bit Parallel Output
1	0	1	0	0	Enables 8 MSB's
1	0	1	0	1	Enables 4 LSB's and 4 Trailing Zeros

TABLE 1, TABLE 2 NOTES:

1. "1" indicates TTL logic high (2.4V minimum).
2. "0" indicates TTL logic zero (0.8V maximum).
3. X indicates "don't care".
4. 0→1, 1→0 indicate logic transitions (edges).
5. Output data format is as follows:

MSB	XXXX	XXXX	XXXX	LSB
	High Bits	Middle Bits	Low Bits	
	8 MSB's		4LSB's	

When initiating a conversion, the signal applied to A_0 (Byte Address/Short Cycle, Pin 4) determines whether a 12-bit conversion is initiated (A_0 = "0") or an 8-bit conversion is initiated (A_0 = "1"). It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0" and A_0 = "1" or "0" that initiates a convert operation, and the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$ as shown in the Truth Table and as described below in the section labeled Timing-Initiating Conversions. When initiating conversions, the 12/$\overline{8}$ line is a "don't care".

When reading digital output data from MN6227/6228, CE and $\overline{CS}$ must be asserted, and the signals applied to 12/$\overline{8}$ and A_0 will determine the format of output data. Logic "1" applied to the R/$\overline{C}$ line will initiate actual output data access. If the 12/$\overline{8}$ line is a "1", all 12 output data bits will be accessed simultaneously when the R/$\overline{C}$ line goes from a "0" to a "1".

If the 12/$\overline{8}$ line is a "0", output data will be accessible as two 8-bit bytes as described below in the section labeled Timing-Reading Output Data. In this situation, A_0 = "0" will result in the 8 MSB's being accessed and A_0 = "1" will result in the 4 LSB's and 4 trailing zeros being accessed. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at one time, as addressed by A_0. For these applications, the 4 LSB's (pins 16-19) should be hardwired to the 4 MSB's (pins 24-27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 though 27. When A_0 goes high, the upper 8 data bits are disabled, the 4 LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 through 23.

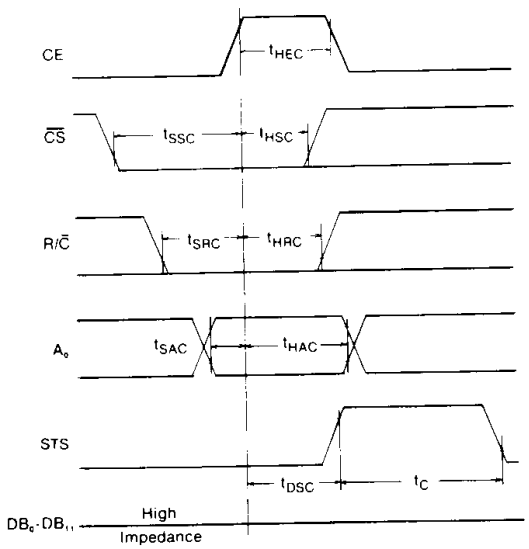
TIMING—INITIATING CONVERSIONS—It is the combination of CE = "1", $\overline{CS}$ = "0", R/$\overline{C}$ = "0" and A_0 = "1" (initiate 8-bit conversion) or A_0 = "0" (initiate 12-bit conversion) that initiates a convert operation. As stated earlier, the actual conversion can be initiated by the rising edge of CE, the falling edge of $\overline{CS}$ or the falling edge of R/$\overline{C}$. The A_0 line should be stable immediately prior to whichever of the above transitions is used to initiate a conversion. The R/$\overline{C}$ transition is normally used to initiate conversions in stand-alone operation, and it is not recommended to use this line to initiate conversion in μP applications. If R/$\overline{C}$ is high just prior to a conversion, there will be a momentary enabling of output data as if a read operation were occuring, and the result could be system bus contention. In most applications, A_0 should be stable and R/$\overline{C}$ low before either CE or $\overline{CS}$ is used to initiate a conversion.

Timing for a typical application is shown below. In this application $\overline{CS}$ is brought low, R/$\overline{C}$ is brought low, and A_0 is set to its chosen value prior to CE becoming a "1". This sequence can be accomplished in a number of ways including connecting $\overline{CS}$ and A_0 to address bus lines, connecting R/$\overline{C}$ to a read/write line (or its equivalent) and generating a CE 0→1 transition using the system clock. In this example $\overline{CS}$ should be a "0" 50nsec prior to the CE transition (t_{SSC} = 50nsec min), R/$\overline{C}$ should be a "0" 50nsec prior to the CE transition (t_{SRC} = 50nsec min), and A_0 should be stable 0nsec prior to the CE transition (t_{SAC} = 0nsec min). The minimum pulse width for CE = "1" is 50nsec (t_{HEC} = 50nsec min) and both $\overline{CS}$ and R/$\overline{C}$ must be valid for at least 50nsec while CE = "1" (t_{HSC} and t_{HRC} = 50nsec min) to effectively initiate the conversion. A_0 must be valid for at least 50nsec (t_{HAC} = 50nsec min) while CE is high to effectively initiate the conversion. The Status Line rises to a "1" no more than 200nsec after the rising edge of CE. (t_{DSC} = 200nsec max). Once the Status = "1", additional convert commands will be ignored until the conversion is complete.

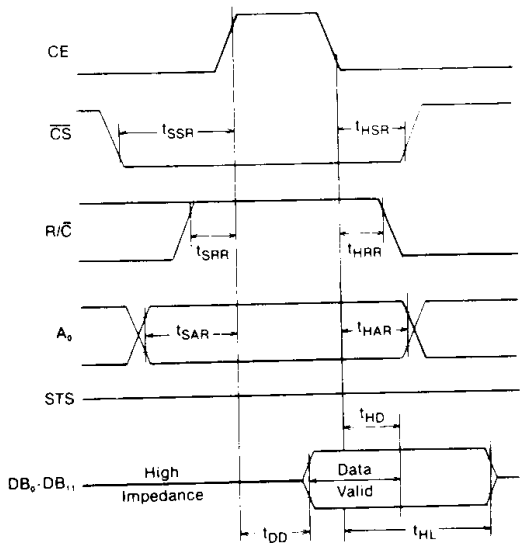
TIMING—RETRIEVING DATA—The combination of CE = "1", $\overline{CS}$ = "0", and R/$\overline{C}$ = "1" is required to access digital output data. If the above combination of control signals is met and the 12/$\overline{8}$ line has a "1" applied, all twelve output bits will become valid simultaneously. If the 12/$\overline{8}$ line has a "0" applied, output data is formatted for an 8-bit data bus, and the 8 MSB's will become valid when the above condition is met with A_0 = "0" while the 8 LSB's (4 data bits and 4 trailing "0's") will become valid whenever A_0 = "1". Data access can be initiated by either the rising edge of CE or the falling edge of $\overline{CS}$.

Timing for a typical application is shown below. In this application, $\overline{CS}$ is brought low, A_0 is set to its final state, and R/$\overline{C}$ is brought high all before the rising edge of CE. $\overline{CS}$ and A_0 should be valid 50nsec prior to CE (t_{SSR} = 50nsec min, t_{SAR} = 50nsec min). R/$\overline{C}$ can become valid the same time as CE (t_{SRR} = 0nsec min). In the 8-bit bus interface mode (12/$\overline{8}$ = "0"), A_0 must be stable at least 50nsec prior to CE going high. A_0 may be toggled at anytime without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in 8-bit bus applications will never be enabled at the same time.

Access time is measured from the point where CE and R/$\overline{C}$ are both high (assuming $\overline{CS}$ is already low).



Convert Start Timing



Read Cycle Timing

MN6227/6228 TIMING SPECIFICATIONS:

CONVERT MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE		100	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low During CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0	0		ns
t_{HAC}	A_0 Valid During CE High	50	20		ns
t_C	Conversion Time				
	8-Bit Cycle	15	13	17	μs
	12-Bit Cycle	10	20	25	μs

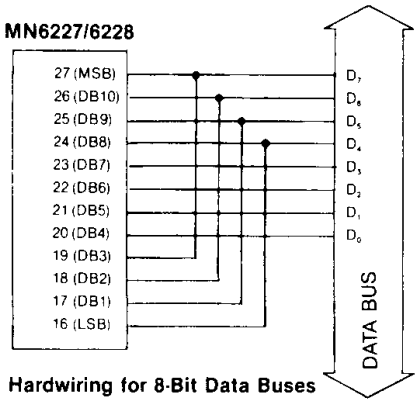
MN6227/6228 TIMING SPECIFICATIONS:

READ MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0	0		ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0	0		ns
t_{HAR}	A_0 Valid After CE Low	50	25		ns

HARDWIRING TO 8-BIT DATA BUSES—For applications with 8-bit data buses, output lines DB4-DB11 (pins 20-27) should be connected directly to data bus lines D_0-D_7. In addition, output lines DB0-DB3 (pins 16-19) should be connected to data bus lines D_4-D_7 or to MN6227/6228 output lines DB8-DB11. Thus, if A_0 is low during a read operation, the upper 8 bits are enabled and become valid on output pins 20-27. When A_0 is high during a read operation, the 4 LSB's are enabled on output pins 16-19 and the 4 middle bits (pins 20-23) are overridden with "0's".

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte ($A_0 = 0$)	MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4
Low Byte ($A_0 = 1$)	DB3	DB2	DB1	DB0	0	0	0	0



Hardwiring for 8-Bit Data Buses

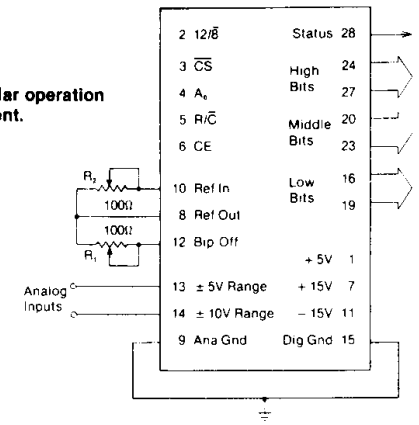
UNIPOLAR OPERATION AND CALIBRATION—Analog input connections and calibration circuits for the unipolar operating mode is shown below. When the 0 to + 10V input range is used, apply the analog input to pin 13 of the MN6227. If gain adjustment is not used, replace trim pot R_2 with a fixed 50Ω ±1% metal-film resistor to meet all published specifications. If unipolar offset adjustment is not used, connect pin 12 (Bipolar Offset) directly to pin 9 (Analog Ground).

Unipolar offset error refers to the accuracy of the 0000 0000 0000 to 0000 0000 0001 digital output transition (see Digital Output Coding). If offset adjustment is not used, this transition will occur within ±2 LSB's of its actual ideal value (+ ½ LSB). For the 10V range, 1 LSB = 2.44mV. To offset adjust, apply an analog input equal to + ½ LSB and with the MN6227 continuously converting, adjust the offset potentiometer "down" until the digital output is all "0's" and then adjust "up" until the LSB just changes from a "0" to a "1". The offset adjust circuit has a range of approximately ±15mV, and different offsets can be set for different system requirements.

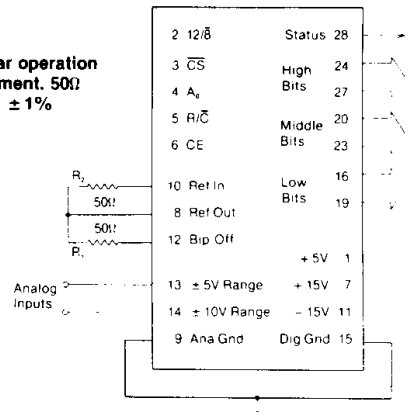
Unipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after unipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal full scale of the selected input range. This voltage is + 9.9963V for the 10V unipolar input range. Gain trimming is accomplished by applying this voltage and adjusting the gain potentiometer "up" until the digital outputs are all "1's" and then adjusting down until the LSB just changes from a "1" to a "0".

If a 10.24V (2.5mV/bit) input range is required, the gain trim pot (R_2) should be replaced with a fixed 50Ω resistor, and a 200Ω trim pot inserted in series with the analog input to pin 13. Offset trimming proceeds the same. Gain trimming is now accomplished with the new pots.

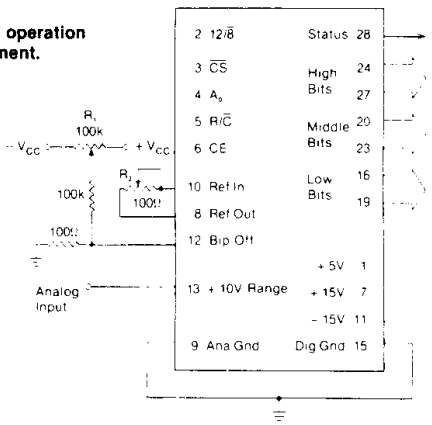
MN6227/6228 bipolar operation with trim adjustment.



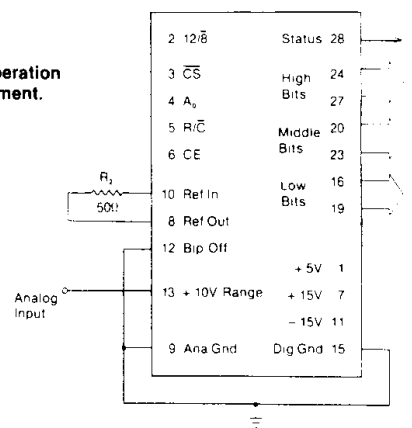
MN6227/6228 bipolar operation without trim adjustment. 50Ω resistors should be ±1% metal film.



MN6227 unipolar operation with trim adjustment.



MN6227 unipolar operation without trim adjustment.



BIPOLAR OPERATION AND CALIBRATION—Analog input connections and calibration circuits for the bipolar operating modes are shown on the previous page. If the ±5V input range is to be used on MN6227, apply the analog input to pin 13. If the ±10V range is to be used on MN6228, apply the analog input to pin 14. If either bipolar offset or bipolar gain adjustment are not to be used, the trim pots R_1 and R_2 can be replaced with fixed 50Ω ±1% metal-film resistors to meet all published specifications.

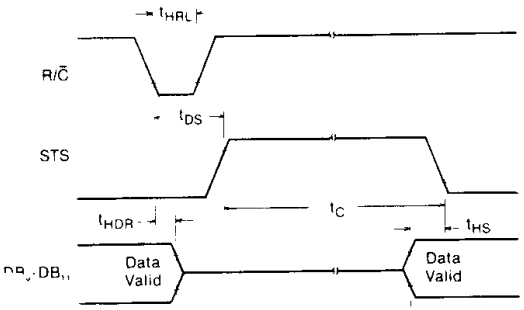
Bipolar zero error refers to the accuracy of the 0111 1111 1111 to 1000 0000 0000 digital output transition (see Digital Output Coding). Ideally, this transition is supposed to occur ½ LSB below zero volts, and if bipolar offset adjustment is not used, the actual transition will occur within the specified limit of its ideal value. Offset adjusting on the bipolar device is performed not at the zero crossing point but at the minus full scale point. The procedure is to apply an analog input equal to −FS + ½ LSB (−4.9988V for the ±5V range, −9.9976V for the ±10V range) and adjust the bipolar offset trim pot "down" until the digital output is all "0's". Then adjust "up" until the LSB just changes from "0" to a "1".

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after bipolar offset adjustment has been accomplished. Ideally, this transition should occur 1½ LSB's below the nominal positive full scale value of the selected input range. This voltage is +4.9963V and +9.9927V respectively for the ±5V and ±10V bipolar input ranges. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trim pot "up" until the digital outputs are all "1's" and then adjusting "down" until the LSB just changes from a "1" to a "0".

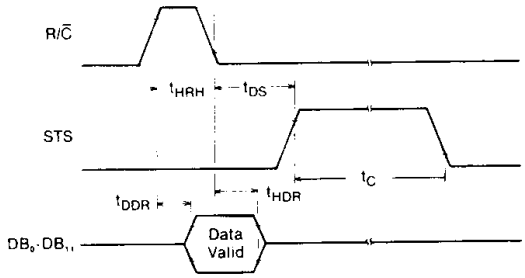
STAND-ALONE OPERATION

The MN6227/6228 can be used in a "stand-alone" mode in systems having dedicated input ports and not requiring full bus interface capability. In this mode, CE and 12/$\overline{8}$ are tied to logic "1", $\overline{CS}$ and A_0 are tied to logic "0", and the conversion is controlled by R/$\overline{C}$. A conversion is initiated when R/$\overline{C}$ is brought low, and all 12 bits of the three-state output buffers are enabled when R/$\overline{C}$ is brought high. This gives rise to two possible modes of operation; conversions can be initiated with either positive or negative R/$\overline{C}$ pulses. The timing diagram below details operation with a negative start pulse. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The Status line goes high 200ns after R/$\overline{C}$ goes low and returns low 300ns after data is valid.

The timing diagram below details operation with a positive start pulse, Output data lines are enabled during the time R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next rising edge of R/$\overline{C}$.



Low Pulse for R/$\overline{C}$—Outputs Enabled After Conversion



High Pulse for R/$\overline{C}$—Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

DIGITAL OUTPUT CODING

ANALOG INPUT VOLTAGE (Volts)			DIGITAL OUTPUT
0 to +10V	±5V	±10V	MSB LSB
+10.0000	+5.0000	+10.0000	1111 1111 1111
+9.9963	+4.9963	+9.9927	1111 1111 111Ø*
+5.0012	+0.0012	+0.0024	1000 0000 000Ø*
+4.9988	−0.0012	−0.0024	0000 0000 000Ø*
+4.9963	−0.0037	−0.0073	0111 1111 111Ø*
+0.0012	−4.9988	−9.9976	0000 0000 000Ø*
0.0000	−5.0000	−10.0000	0000 0000 0000

DIGITAL OUTPUT CODING NOTES:

1. For unipolar input range, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +10V or ±5V input ranges, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
4. For ±10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN6228 operating on its ±10V input range, the transition from digital output 0000 0000 0000 to 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.9976 volts. Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of −0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".